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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/527,873	03/17/00	SHOOSHTARIAN S	AGX-37

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EXAMINER	
LEE,H	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 02/14/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/527,873	Shooshtarian et al.
Examiner	**Group Art Unit**
Hsien-Ming L	2823

☒ Responsive to communication(s) filed on *Jan 8, 2001*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-13* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-13* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *5*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. The cancellation to claims 14-41 is acknowledged. Thus, claims 1-13 are now pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

3. Claims 1-2, 6-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Colelli et al. (US 6,100,506).

Colelli et al. teach a method for heat treating a semiconductor wafer using an in-situ closed loop real-time hot plate surface temperature monitoring system which also includes a characterization and adjustment system for controlling the hot plate surface temperature across various zones thereof (col. 2, line 20 through col. 8, line 11), comprising the steps of:

* placing a semiconductor in a thermal processing chamber, said semiconductor wafer defining at least one localized region along a radical axis;

* adjusting the temperature of said semiconductor wafer to a predetermined temperature according to a heat cycle which includes a heating stage (col. 2, lines 49-53; col. 2, line 60 through col. 3, line 9; col. 3, lines 56-64);

* during at least one stage of said heat cycle, controlling the localized temperature of said at least one localized region of said semiconductor wafer to minimize temperature deviation to be less than 0.3 C across the wafer from predetermined temperature (col. 3, lines 15-17; col. 3, 48-51; col. 5, lines 6-14 and lines 24-34).

The method further comprising the steps of monitoring the temperature of said at least one localized region with a temperature sensing device, said temperature sensing device being communication with a controller; and based on the information received by said controller from said temperature sensing device, controlling the temperature of said at least one localized region according to said heat cycle (figs 1-3 and col. 2, lines 49-53; col. 3, line 65 through col. 14).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Chiba (US 4,924,073).

Chiba teaches a method for heat treating a semiconductor wafer, comprising the steps of :

* placing a semiconductor in a thermal processing chamber, said semiconductor wafer defining at least one localized region along a radical axis (fig. 1A);

* adjusting the temperature of said semiconductor wafer to a predetermined temperature according to a heat cycle which includes a heating stage (fig. 2);

* during at least one stage of said heat cycle, controlling the localized temperature of said at least one localized region of said semiconductor wafer to minimize temperature deviation from predetermined temperature (col. 5, lines 9-32 ; col. 9, lines 19-26; col.).

The method further comprising the steps of monitoring the temperature of said at least one localized region with a temperature sensing device, said temperature sensing device being communication with a controller; and based on the information received by said controller from said temperature sensing device, controlling the temperature of said at least one localized region according to said heat cycle (figs. 1A, 1C, 4, 6, 8, 10).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Champetier et al. (US 5,997,175).

Champetier substantially teach the claimed method for heat treating a semiconductor wafer, said method comprising the steps of :

* placing a semiconductor 14 in a thermal processing chamber 12, said semiconductor wafer 14 defining at least one localized region along a radical axis (fig. 1);

* adjusting the temperature of said semiconductor wafer to a predetermined temperature according to a heat cycle which includes a heating stage, i.e. measuring a semiconductor wafer temperature by reflecting thermal radiation being emitted by a surface of the wafer and then sensing the reflected radiation at a plurality of locations wafer through pyrometers with the assistance of a control system for the purpose of adjusting the wafer temperature (summary of the invention);

* during at least one stage of said heat cycle, controlling the localized temperature of said at least one localized region of said semiconductor wafer, i.e. during the stage of heat treating, controlling the localized temperature of plural locations of wafer through a control system in communication with the radiation sensing devices and with the heat source, wherein the controller can be configured to receive thermal radiation information from the radiation sensing device and, based on the information to control the amount of heat being emitted by the heat source which in turn to control localized temperature of said wafer (col. 4, line 50 through col.5, line 3).

The method further comprising the steps of monitoring the temperature of said at least one localized region with a temperature sensing device such as pyrometer, said temperature sensing device being communication with a controller; and based on the information received by said controller from said temperature sensing device, controlling the temperature of said at least one localized region according to said heat cycle (col. col. 4, line 50 through col.5, line 3 ; col. 17,

lines 19-61). The method also further comprises the steps of providing a gas to control the temperature of the wafer (fig. 1 and col. 7, lines 34-40); the step of controlling the temperature and the flow rate of said gas (col. 11, lines 47-58).

Champertier does not expressly teach controlling the localized temperature of the wafer for the purpose of minimizing temperature deviation. Nevertheless, Champetier teaches controlling the wafer temperature by rotating the wafer for promoting greater temperature uniformity (col. 7, lines 49-53), i.e decrease temperature fluctuation at the plural locations of the wafer. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to appreciate that Champetier's teaching implies the minimization of temperature deviation can be achieved by rotating the wafer.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is (703) 305-7341. The examiner can normally be reached on Monday-Friday from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918. The fax phone number for this Group is (703) 305-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hsien-Ming Lee

Examiner Group 2823

Feb. 9, 2001

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800